Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.043”**

**.071”**

**1**

**10**

**9**

**8**

**2**

**3 4 5 6 7**

**3**

**5**

**B**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: 35B**

**APPROVED BY: DK DIE SIZE .043” X .071” DATE: 11/9/21**

**MFG: NATIONAL SEMI THICKNESS .016” P/N: LM35**

**DG 10.1.2**

#### Rev B, 7/19/02